



## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 1672

SERIAL NUMBER 10/042,732	FILING DATE 04/25/2001  RULE	CLASS 438	GROUP ART UNIT 2813	ATTORNEY DOCKET NO. 039153-0433 (C167596-CIP)
-----------------------------	---------------------------------------	--------------	------------------------	--

## APPLICANTS

Craig S. Sander, Mountain View, CA;

Rich K. Klein, Mountain View, CA;

Asim A. Selcuk, Cupertino, CA; Nicholas J. Kepler, San Jose, CA;

Christopher A. Spence, Sunnyvale, CA;

Raymond T. Lee, Sunnyvale, CA;

John C. Holst, San Jose, CA;

Stephen C. Horne, Austin, TX;

## \*\* CONTINUING DATA \*\*\*\*\*

This application is a DIV of 09/515,875 02/29/2000 PAT 6,287,953  
 which is a CIP of 09/119,934 07/21/1998 PAT 6,146,954

*TN*  
 \*\* FOREIGN APPLICATIONS \*\*\*\*\* *Nme*

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

\*\* 03/27/2003

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	STATE OR	SHEETS	TOTAL	INDEPENDENT
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged	CA	5	20	3
Examiner's Signature <i>T.N.</i> Initials				

## ADDRESS

Joseph N. Ziebert  
 FOLEY & LARDNER  
 Firststar Center  
 777 East Wisconsin Avenue  
 Milwaukee, WI  
 53202-5367

## TITLE

Minimizing transistor size in integrated circuits